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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/829,136	04/21/2004	Hee-hwan Choe	8116-1 (PL0026/US)	5461

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EXAMINER	
DHINGRA, RAKESH KUMAR	
ART UNIT	**PAPER NUMBER**
1763	

DATE MAILED: 02/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/829,136	CHOE ET AL.	
	Examiner	Art Unit	
	Rakesh K. Dhingra	1763	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Response to Arguments

Applicant's arguments with respect to claims 1-7 have been considered but are moot in view of the new ground(s) of rejection as explained below:

Rejections under 35 USC 102

Claims 1, 3, 5 (Suemasa et al)

Applicant has amended independent claim 1 by adding new limitations. Further applicant argues that Suemasa et al do not disclose or suggest a mixed voltage comprising E1cos(w1t) for generating plasma and E1+(E2-E1)cos(w2t) for adjusting etching conditions (as per amended claim 1 limitation); in contrast Suemasa et al disclose single frequencies of 380 Khz, 3 Mhz and 13.56 Mhz respectively applied to a lower electrode. Thus claim 1 is not anticipated by Suemasa et al and its rejection should be withdrawn. Further since claims 3, 5 depend upon claim 1, these are also not anticipated by Suemasa et al.

Examiner responds that Suemasa et al teaches application of superimposed power of two frequencies to lower electrode 106, which implies combining or mixing the power from two power supply sections 114, 116 (Paragraph 0020). In this regard, Suemasa et al also teaches that higher plasma density is obtained in case of superimposed power of two frequencies as against the case when two single frequencies are separately applied to lower the electrode (Figure 3 and Paragraph 0035). Examiner further responds that since reference by Suemasa et al teaches the amended claim 1 limitations, it has been rejected under 35 USC 102 as explained below. For that reason rejection of dependent claims 3, 5 has also been maintained under 35 USC 102 (e) as explained below.

Examiner also responds that an additional new reference by Wikuramanayaka (JP Pub. No. 2002-246368) has been found that reads on amended claim 1 limitations and accordingly claim 1 and dependent claims 3, 5 have been rejected under 35 USC 102(e).

Rejections under 35 USC 103(a)

Claims 1-7 (Donohoe et al in view of Quon et al)

Applicant has amended independent claim 7 by adding new limitations.

Further applicant argues that amendments to claims 1, 7 render the claims 1-7 patentable over the cited references since Donohoe et al and Quon et al when taken alone or in combination fail to teach or suggest a mixed voltage comprising E1cos(w1t) for generating plasma and E1+(E2-E1)cos(w2t) for adjusting etching conditions as recited in amended claims 1, 7. Thus claims 1, 7 are patentable over Donohoe et al in view of Quon et al. Further claims 2-6 being dependent claims are also patentably distinct over the cited references.

Examiner responds that Donohoe et al in view of Quon et al read on the amended claims 1, 7 as explained below. According claims 1, 7 have been rejected under 35 USC 103(a) as explained below. Further claims 2-6 being dependent claims have also been rejected as explained below.

Claims 2, 4, 6 and 7 (Suemasa et al in view of Donohoe et al)

Applicant argues that Suemasa et al and Donohoe et al when taken alone or in combination fail to teach or suggest mixed voltage comprising E1cos(w1t) for

generating plasma and E1+(E2-E1)cos(w2t) for adjusting etching conditions as already given under claims 1, 7 and therefore rejection of claims 2, 4, 6, 7 should be withdrawn.

Examiner responds that for the reasons given above and further as explained below claims 2, 4, 6, 7 stand rejected as being unpatentable over Suemasa et al in view of Donohoe et al.

DETAILED ACTION

Claim Rejections - 35 USC § 102

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 3, 5 are rejected under 35 U.S.C. 102 (b) as anticipated by Suemasa et al (US PGPUB No. 2003/0054647).

Regarding Claim 1: Suemasa et al teach a plasma processing apparatus 100 (Figure 1) comprising:

a processing chamber 102 with a lower electrode 106 and an upper electrode 108;

a first high frequency power supply (main power supply) 114 comprising a first power source 122 to generate a main voltage having a predetermined main frequency and a predetermined amplitude, and a first impedance matching circuit to impedance-match the main voltage;

a second high frequency power supply (bias power supply) 116 comprising a bias power source 128 to generate a bias voltage having a predetermined bias frequency

and a predetermined amplitude and a second impedance matching circuit to impedance-match the bias voltage; and

a power supply device (mixer) 112 that receives and superimposes (mixes) the main voltage and the bias voltage, and outputs the mixed voltage through respective matching circuits 120, 126 to the lower electrode 106 (Paragraphs 0019, 0020, 0035). Suemasa et al further teach that by properly adjusting the first and second high frequency power components the plasma density and self-bias can be adjusted to realize desired plasma processing (Paragraph 0036).

The mixed voltage would thus inherently include a portion for generating plasma that would depend upon the amplitude and frequency of the main voltage and another portion for adjusting the process (etching) condition as per equation given on page 9, lines 2, 3 of the specification.

Regarding Claim 3: Suemasa et al teach that the power supply device 112 superimposes (combines/mixes) the outputs of the first and second high frequency power supplies 114 and 116 and which is then coupled to the lower electrode 106 for supplying a superimposed power of the two frequencies coming from the first and second high frequency power supplies 122, 128 respectively (Paragraphs 0020, 0035).

Regarding Claim 5: Suemasa et al teach a second high frequency supply 116 for producing a high frequency power component, which is lower than the first high frequency power component supplied by the first high frequency power supply 114 (Paragraph 0020).

Claims 1, 3, 5 are rejected under 35 U.S.C. 102 (b) as anticipated by Wikuramanayaka (JP Pub. No. 2002-246368).

Regarding Claim 1: Wikuramanayaka teaches a plasma processing apparatus (Figure 1) comprising:

a reaction container (processing chamber) 10 with an RF (lower) electrode 16 and a gas installation plate (grounded showerhead -like upper electrode) 18;

a first RF generator (main power supply) 31 to generate a main voltage having a predetermined main frequency and a predetermined amplitude, and a first impedance matching circuit 33 to impedance-match the main voltage;

a second RF generator (bias power supply) 32 to generate a bias voltage having a predetermined bias frequency and a predetermined amplitude and a second impedance matching circuit 34 to impedance-match the bias voltage; and

a high frequency mixer 35 connected to both impedance matching circuits 33, 34 that receives and mixes the main voltage and the bias voltage, and outputs the mixed voltage to the lower electrode 16 (Paragraph 0034).

Wikuramanayaka further teaches that by properly selecting high and low frequencies plasma production and acceleration of ions can be controlled (Paragraph 0034).

The mixed voltage would thus inherently include a portion for generating plasma that would depend upon the amplitude and frequency of the main voltage and another portion for adjusting the process (etching) condition as per equation given on page 9, lines 2, 3 of the specification.

Regarding Claim 3: Wikuramanayaka teaches that the high frequency mixer 35 combines the outputs of the first and second RF generators 31, 32 supplies 114 and 116 by superimposing (adding) and which is then coupled to the lower electrode 106 for supplying a superimposed power of the two frequencies coming from the first and second high frequency power supplies 122, 128 respectively (Paragraphs 0020, 0035).

Regarding Claim 5: Wikuramanayaka teaches that frequency of one RF generator is in VHF range and of the other one is in HF range (Paragraphs 0022, 0034).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to

consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1-7 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Donohoe et al (US Patent No. 6,309,978 B1) in view of Quon et al (Pub No. US 2003/0094239 A1).

Regarding Claim 1: Donohoe et al teach a plasma chamber 101 (Figure 4) comprising a lower electrode 102 and an upper electrode 103, and used for etching/deposition comprising:

a multi-frequency RF source 114 connected to lower electrode 102 (Column 5, lines 20-38). Donohoe et al further teach that the multi-frequency source 114 (per Figure 6) includes three frequency generators 31, 32, 33 and which provide discrete (predetermined) frequency and discrete power (predetermined amplitude) levels (Figure 7 and Column 6, lines 14-17). Donohoe et al also teach that apparatus further includes a mixer 37 which combines the output signals of three frequency generators 31, 32, 33 and provides output signal 30 (having a beat component) to the lower electrode 102. Donohoe et al also teach various generators 31, 32, 33 can provide a spectrum of frequencies /power levels (Column 6, lines 5-25).

Donohoe et al do not teach impedance matching circuits.

Quon et al teach a plasma apparatus 20 (Figure 3A) comprising a process chamber with a wafer supporting chuck (Lower electrode) 18;

a very high frequency generator 14 and a VHF match network 30;

a low frequency RF generator 16 (for bias) and a low frequency RF match network 32;

a combiner circuit (mixer) 34 that adds (superposes) the respective RF and VHF signals and a coupling circuit 12 which combines the VHF and the RF signals at the chuck, while maintaining impedance match between VHF and RF generators and the load (Paragraphs 0022, 0023, 0024).

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to use impedance matching circuits as taught by Quon et al in the apparatus of Donohoe et al to provide a matched RF signal to the lower electrode (Paragraph 0024).

The mixed voltage would inherently include a portion for generating plasma that would depend upon the amplitude and frequency of the main voltage and another portion for adjusting the process (etching) condition as per equation given on page 9, lines 2, 3 of the specification.

Regarding Claim 2: Donohoe et al teach that plasma generation is facilitated by the multi-frequency RF source 114 that includes three frequency generators 31, 32, 33 whose frequencies interfere with each other to produce beat which produces a modulated-bias plasma and the multi-frequency RF source includes a mixer 37 which combines the output of three frequency generators 31, 32, 33 and supplies the output signal 30 to the lower electrode 102 (Figures 4, 6, 7 and Column 5, lines 25-30).

Regarding Claims 3, 4: Donohoe et al teach that for mixer 37, summing junction (adding) is preferred for the high frequencies used for plasma generation (Column 6, lines 30-35).

Regarding Claims 5, 6: Donohoe et al also teach (Figure 7) that the three frequencies can be different.

Regarding Claim 7: Donohoe et al in view of Quon et al teach all limitations of the claim including filters in the combiner circuit (mixer) 34 that prevent the main power source and the bias power source from being directly connected to the lower electrode for simultaneously supplying AC power from the main and bias power sources to the lower electrode (Quon et al - Paragraph 0024).

Claims 2, 4, 6, 7 are rejected under 35 U.S.C. (a) as being unpatentable over Suemasa et al (US PG Pub. No. 2003/0054647) in view of Donohoe et al (US Patent No. 6,309,978 B1).

Regarding Claim 2: Suemasa et al teach all limitations of claim 1 (as explained above) except for the auxiliary power supply.

Donohoe et al teach a plasma generation apparatus (Figure 4) comprising a process chamber 101 with a pair of RF electrodes 102, 103, showing the lower electrode 102 connected to a multi-frequency RF source 114 that includes a mixer 37, which combines the output of three frequency generators 31, 32, 33 to provide the output signal 30 which is coupled to the lower electrode 102 (Figure 6 and Column 6, lines 6-14).

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to utilize three frequencies to produce beat and produce a modulated-bias plasma, as taught by Donohoe et al in the apparatus of Suemasa et al to enable a more

efficient process due to higher ion energy for etching and improvement in power consumption.

Regarding Claim 4: Donohoe et al teach that for mixer 37 summing junction (adding) is preferred for the high frequencies used for plasma generation (Figure 6 and Column 6, lines 30-35).

Regarding Claim 6: As explained above, Donohoe et al also teach (per Figure 7) that the three frequencies can be different.

Regarding Claim 7: Donohoe et al in view of Suemasa et al teach all limitations of the claim including filters circuits 118, 124 in the power supply (mixer) 112 that prevent the main power source and the bias power source from being directly connected to the lower electrode for simultaneously supplying AC power from the main and bias power sources to the lower electrode (Suemasa et al - Paragraphs 0020, 0036).

Claims 2, 4, 6 are rejected under 35 U.S.C. (a) as being unpatentable over Wikuramanayaka (JP Pub. No. 2002-246368) in view of Donohoe et al (US Patent No. 6,309,978 B1).

Regarding Claim 2: Wikuramanayaka teaches all limitations of claim as explained above except for the auxiliary power supply.

Donohoe et al teach a plasma generation apparatus (Figure 4) comprising a process chamber 101 with a pair of RF electrodes 102, 103, showing the lower electrode 102 connected to a multi-frequency RF source 114 that includes a mixer 37, which combines the output of three frequency generators 31, 32, 33 to provide the output

signal 30 which is coupled to the lower electrode 102 (Figure 6 and Column 6, lines 6-14).

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to utilize three frequencies to produce beat and produce a modulated-bias plasma, as taught by Donohoe et al in the apparatus of Wikuramanayaka to enable a more efficient process due to higher ion energy for etching and improvement in power consumption.

Regarding Claim 4: Donohoe et al teach that for mixer 37 summing junction (adding) is preferred for the high frequencies used for plasma generation (Figure 6 and Column 6, lines 30-35).

Regarding Claim 6: As explained above, Donohoe et al also teach (per Figure 7) that the three frequencies can be different.

Claim 7 is rejected under 35 U.S.C. 103 (a) as being unpatentable over Wikuramanayaka (JP Pub. No. 2002-246368) in view of Quon et al (Pub No. US 2003/0094239 A1).

Regarding Claim 7: Wikuramanayaka teaches all limitations of the claim including:

a reaction container (processing chamber) 10 with an RF (lower) electrode 16 and a gas installation plate (grounded showerhead -like upper electrode) 18;

a first RF generator (main power supply) 31 to generate a main voltage having a predetermined main frequency and a predetermined amplitude, and a first impedance matching circuit 33 to impedance-match the main voltage;

a second RF generator (bias power supply) 32 to generate a bias voltage having a predetermined bias frequency and a predetermined amplitude and a second impedance matching circuit 34 to impedance-match the bias voltage; and

a high frequency mixer 35 connected to both impedance matching circuits 33, 34 that receives and mixes the main voltage and the bias voltage, and outputs the mixed voltage to the lower electrode 16 (Paragraph 0034).

Wikuramanayaka also teaches that by properly selecting high and low frequencies plasma production and acceleration of ions can be controlled (Paragraph 0034).

The mixed voltage would thus inherently include a portion for generating plasma that would depend upon the amplitude and frequency of the main voltage and another portion for adjusting the process (etching) condition as per equation given on page 9, lines 2, 3 of the specification.

Wikuramanayaka does not teach that mixer prevents the main power source and the bias power source from being directly connected to the lower electrode for simultaneously supplying AC power from the main and bias power sources to the lower electrode.

Quon et al teach a plasma apparatus 20 (Figure 3A) comprising a process chamber with a wafer supporting chuck (Lower electrode) 18;

a very high frequency generator 14 and a VHF match network 30;

a low frequency RF generator 16 (for bias) and a low frequency RF match network 32;

a combiner circuit (mixer) 34 that adds (superposes) the respective RF and VHF signals and a coupling circuit 12 which combines the VHF and the RF signals at the chuck,

while maintaining impedance match between VHF and RF generators and the load (Paragraphs 0022, 0023, 0024). Quon et al also teach that filters in the combiner circuit (mixer) 34 prevents the main power source and the bias power source from being directly connected to the lower electrode for simultaneously supplying AC power from the main and bias power sources to the lower electrode (Paragraph 0024).

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to use impedance matching circuits as taught by Quon et al in the apparatus of Wikuramanayaka to provide a matched RF signal to the lower electrode (Paragraph 0024).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

Aoki et al (US Patent No. 6,861,373) teach a plasma apparatus (Figures 1C, 2) where three high frequency power supplies 321, 322, 323 are connected to matching box 341 through respective filters 331, 332, 333 and where the synthesized power of the three power supplies is coupled to upper electrode 2114 (Column 14, line 40 to Column 16, line 20).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Rakesh K. Dhingra whose telephone number is (571)-272-5959. The examiner can normally be reached on 8:30 -6:00 (Monday - Friday). If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Parviz Hassanzadeh can be reached on (571)-272-1435. The fax phone

number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Rakesh K Dhingra

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